

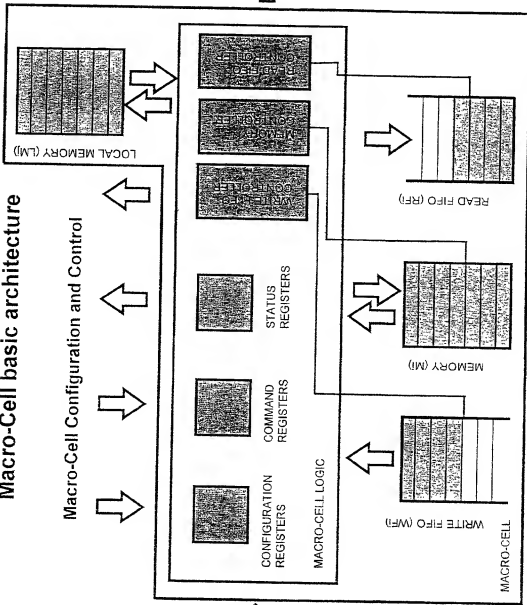
Figure 1

# Macro-Cell basic architecture

## Macro-Cell Configuration and Control

Primary Inputs

Primary Outputs



Prior Art

Figure 2

## BUS BASED MULTI BOARD ARCHITECTURE

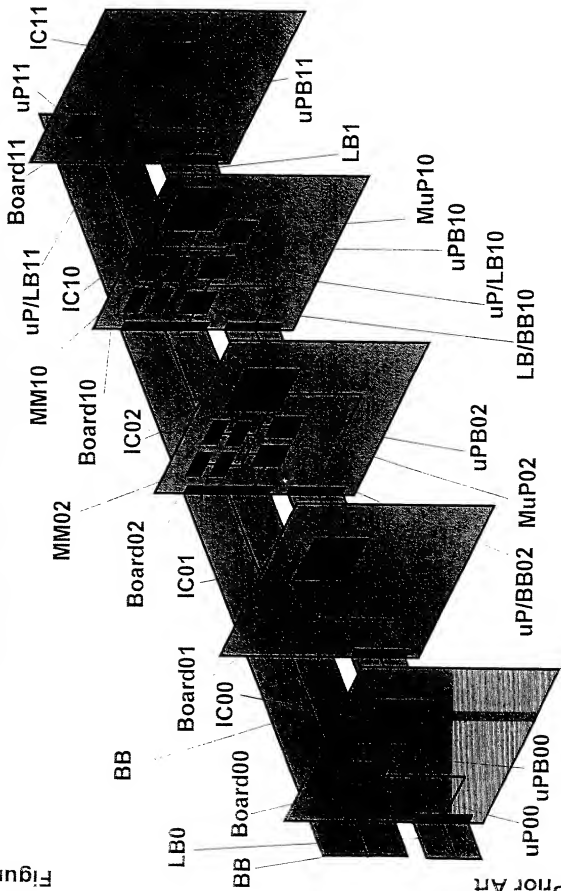
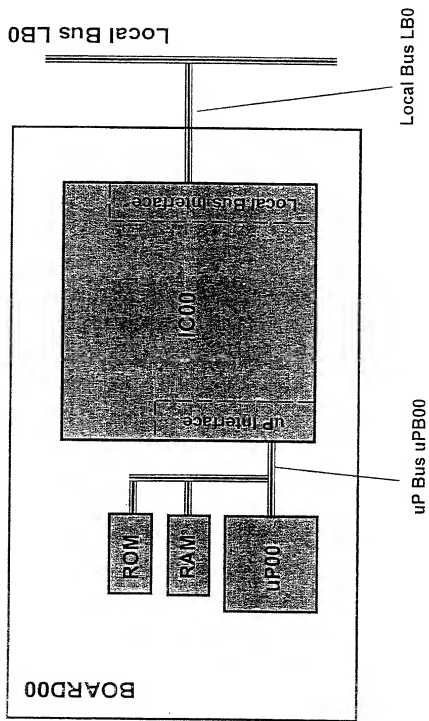


Figure 3

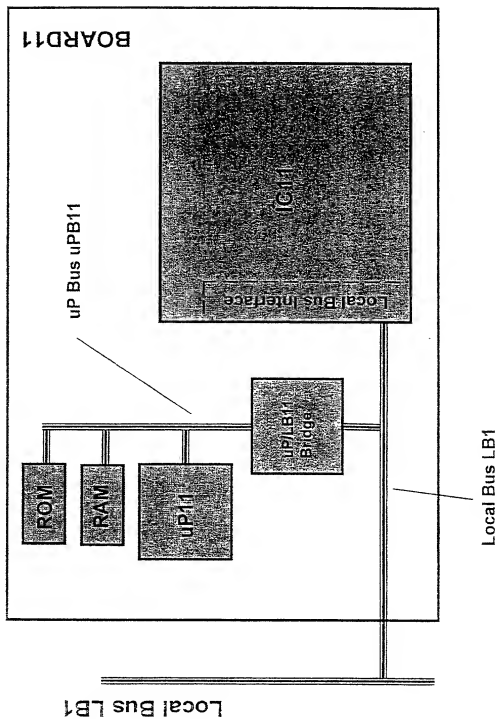
## IC WITH uP INTERFACE AND LOCAL BUS INTERFACE



Prior Art

Figure 4

## IC WITH LOCAL BUS INTERFACE

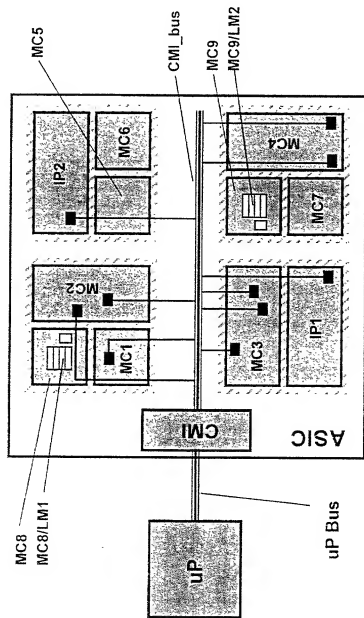


Prior Art



Figure 6

# ASIC implementation of CMI with CBI macro-cells interface



Prior Art

- Cluster of macro-cells
- Registers
- RFi/WFi/Mi/LMi
- RFi/WFi/Mi/LMi controller

Figure 7

# ASIC implementation of CLB with CBL macro-cells interface

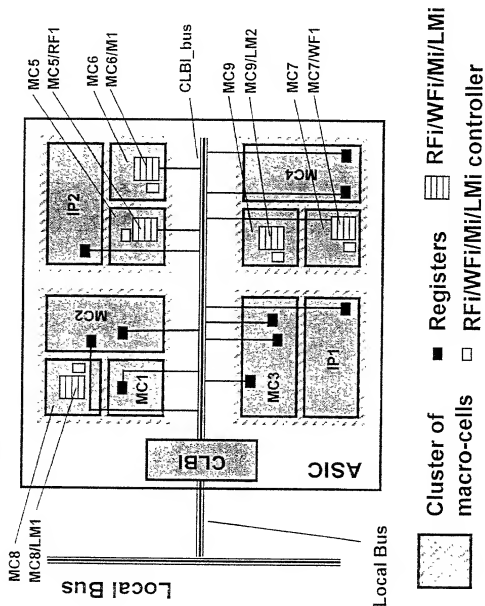






Figure 9

## Board hosting ASIC implementation of AAL5 interfaced via DMI

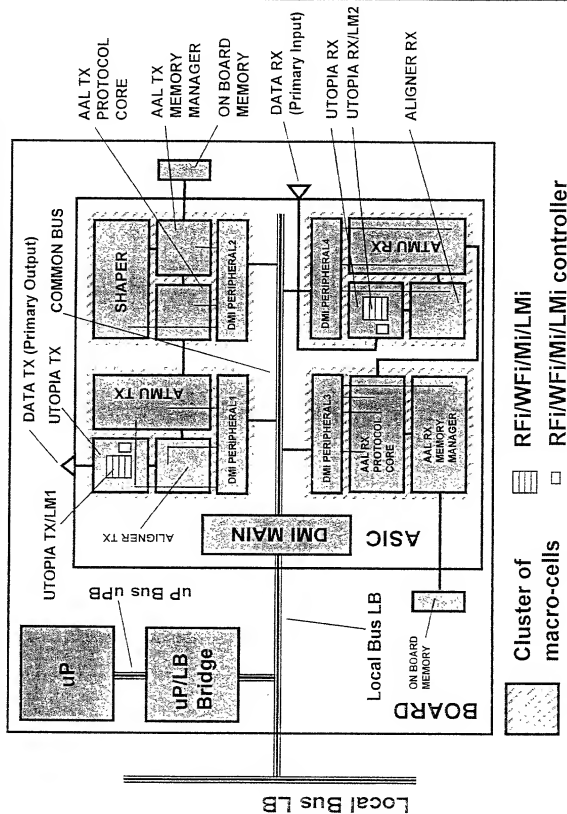


Figure 10

Board hosting FPGA bread-boarding implementation  
of a DMI for microprocessor interface and a DMI for local bus interface

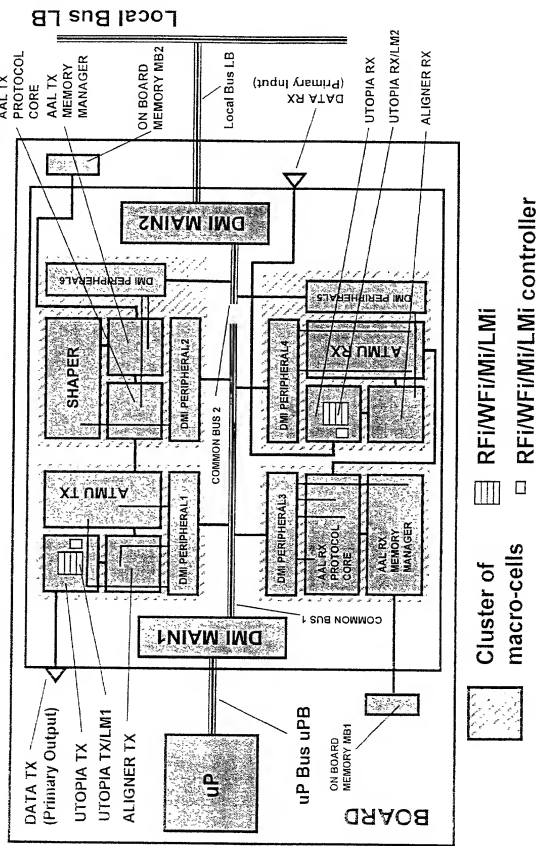


Figure 11

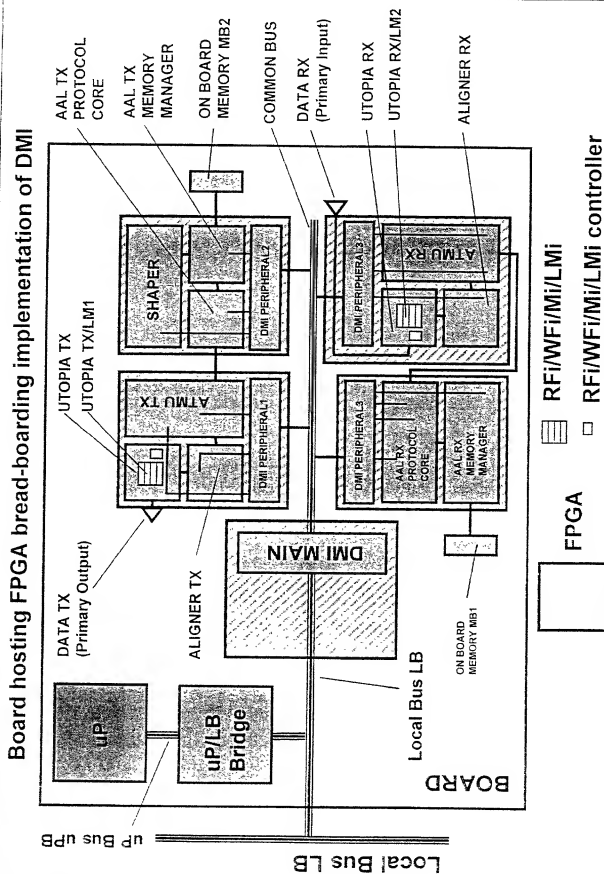


Figure 12

## COMMON BUS exploded in sub-buses

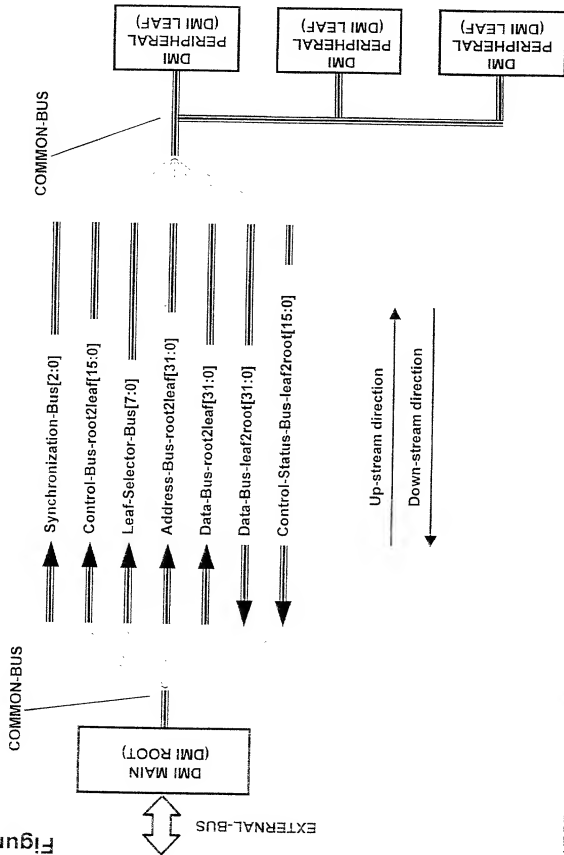


Figure 13

## Common bus exploded in sub-buses

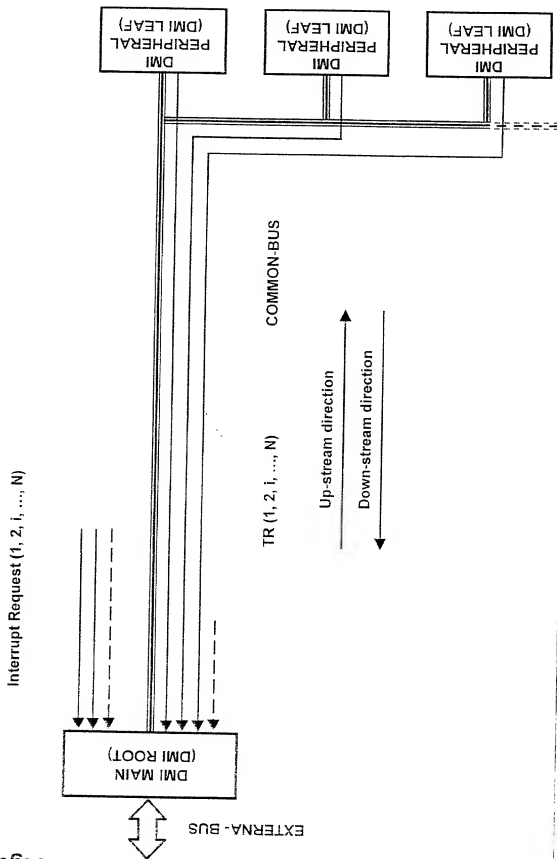




Figure 15

## DMI compliant macro-cell basic architecture

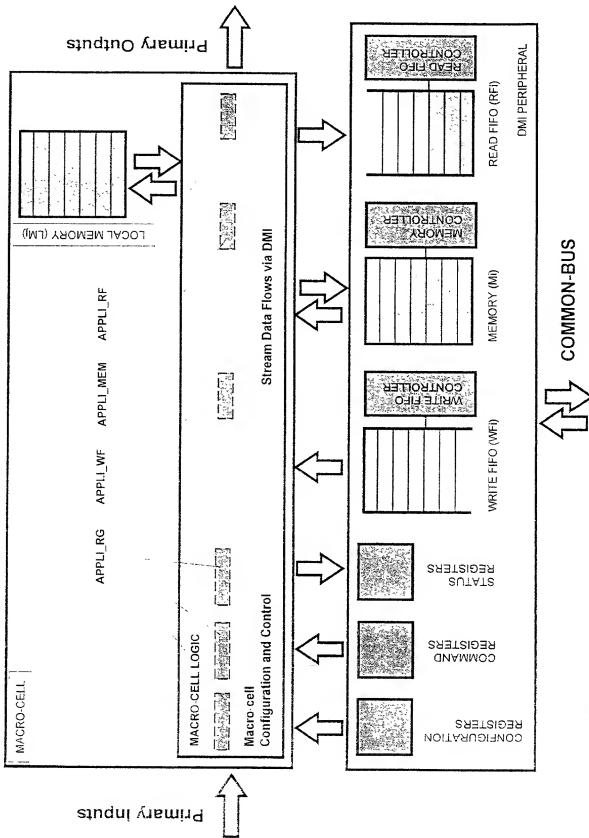


Figure 16

# DMI PERIPHERAL Shadowed Layers

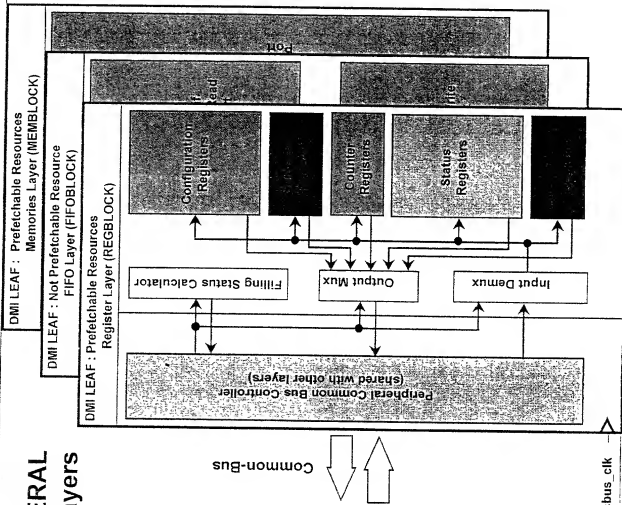




Figure 17

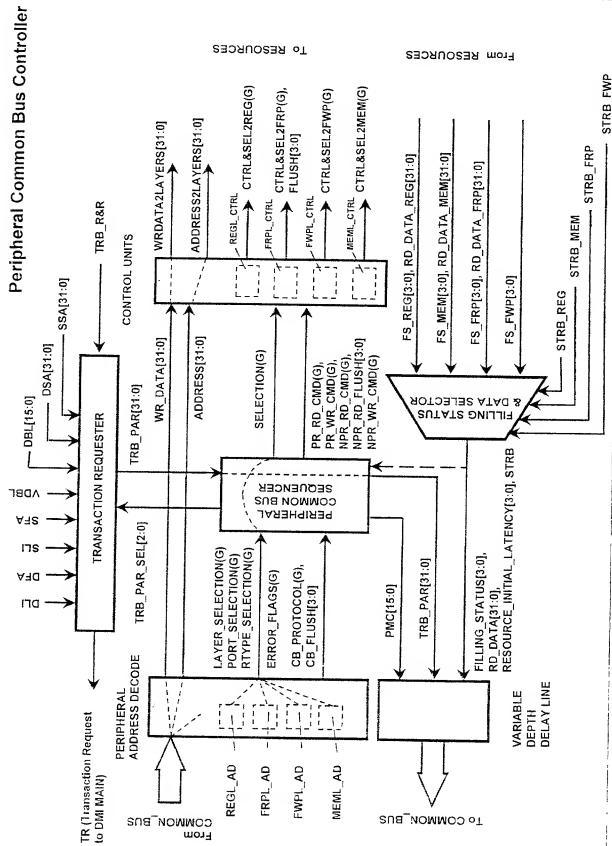
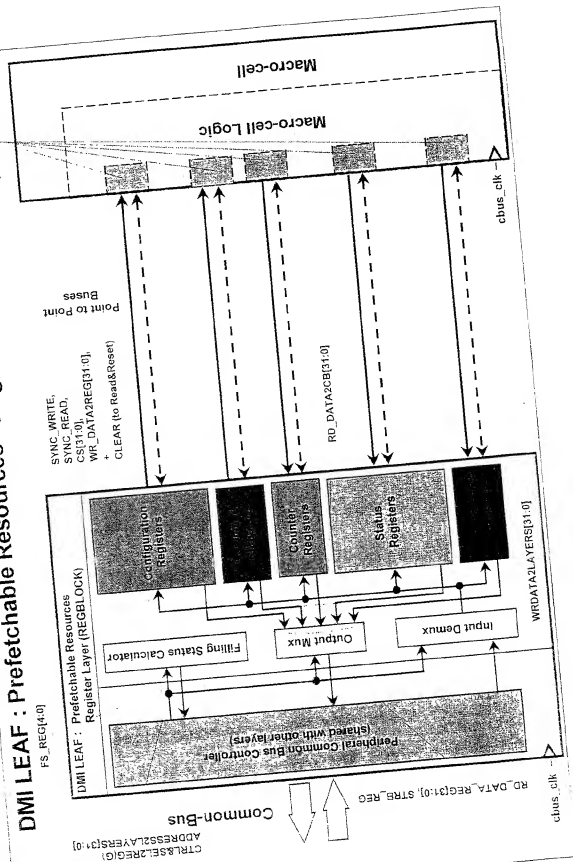


Figure 18

## 4.1 Resources - Registers Layer (REGBLOCK)



# DMI LEAF : Prefetchable Resources - Registers Layer (REGBLOCK)

Figure 19

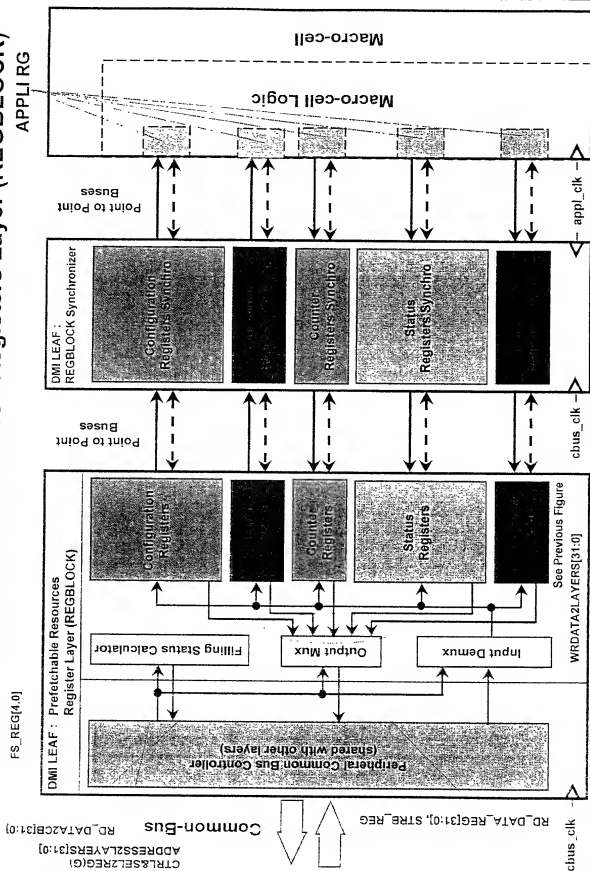
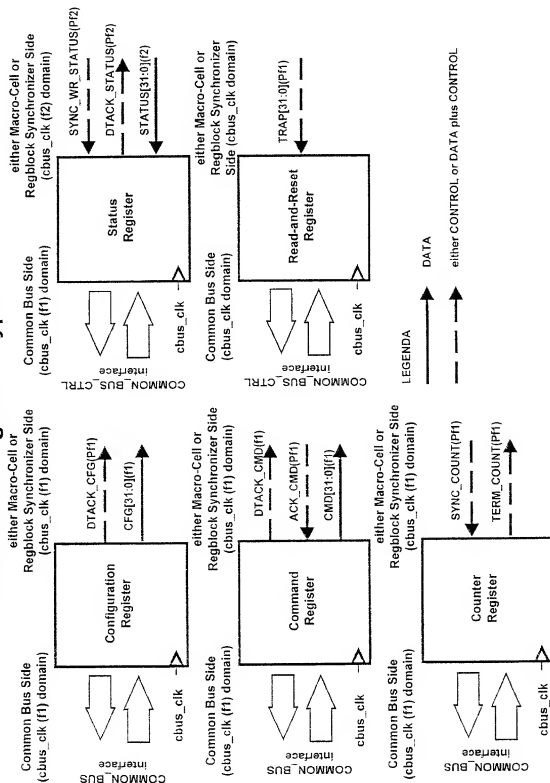


Figure 20

## REGBLOCK Registers Types



NOTE: *DATA\_FROM\_CB[31:0]* is *THRESHOLD[31:0]*  
*DATA2xCB[31:0]* is *COUNTER[31:0]*

Figure 21

# REGBLOCK SYNCHRONIZER Register Synchronizer Types

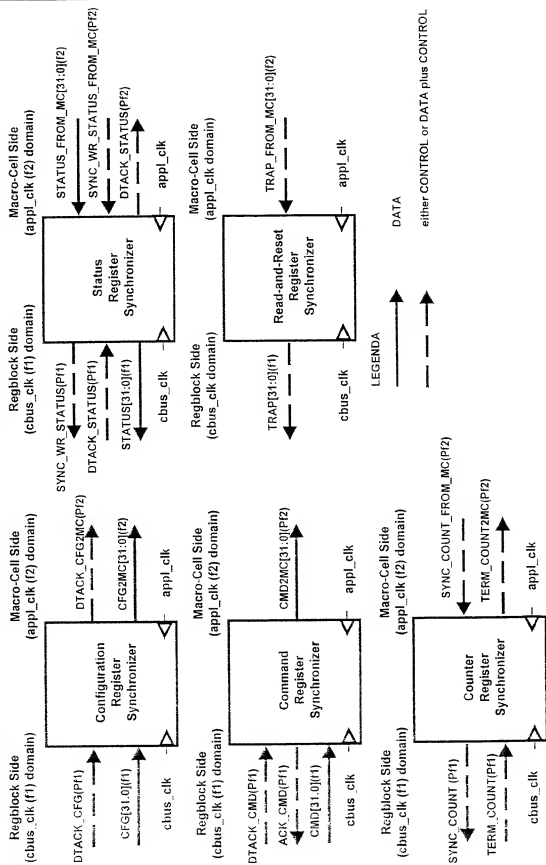
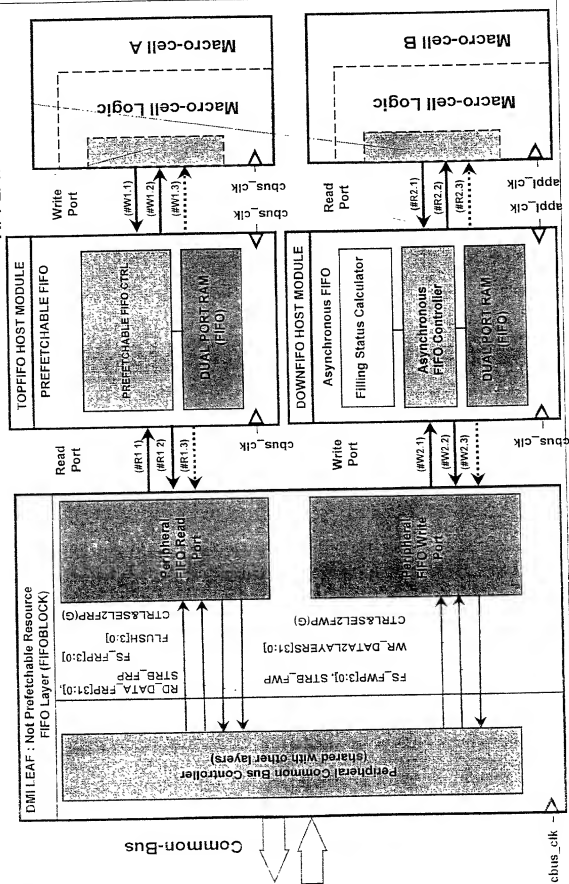


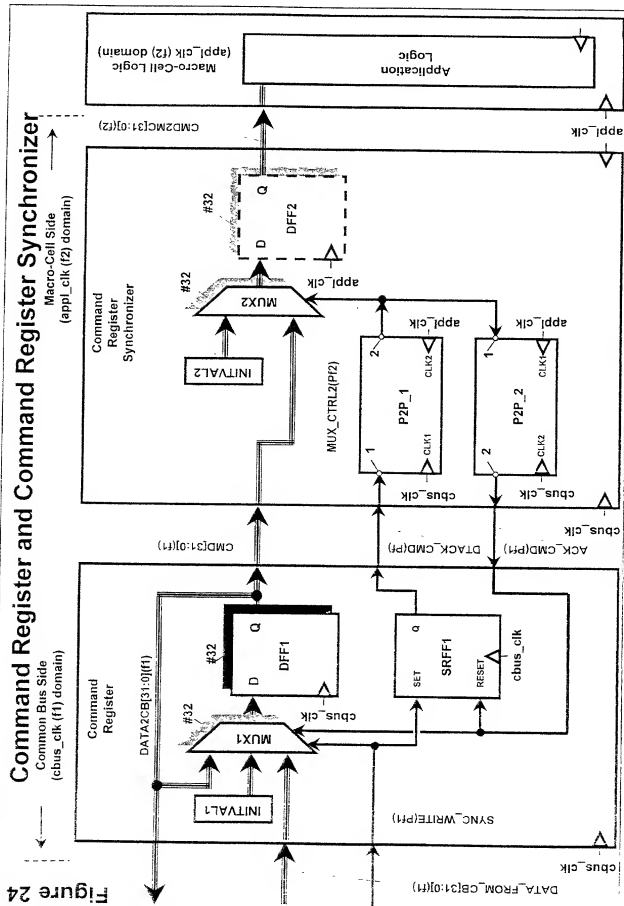


Figure 23

# DMI LEAF : Not Prefetchable Resources FIFO Layer (FIFOBLOCK)

APPLI WF APPLI RF







# Status Register and Status Register Synchronizer

Figure 25

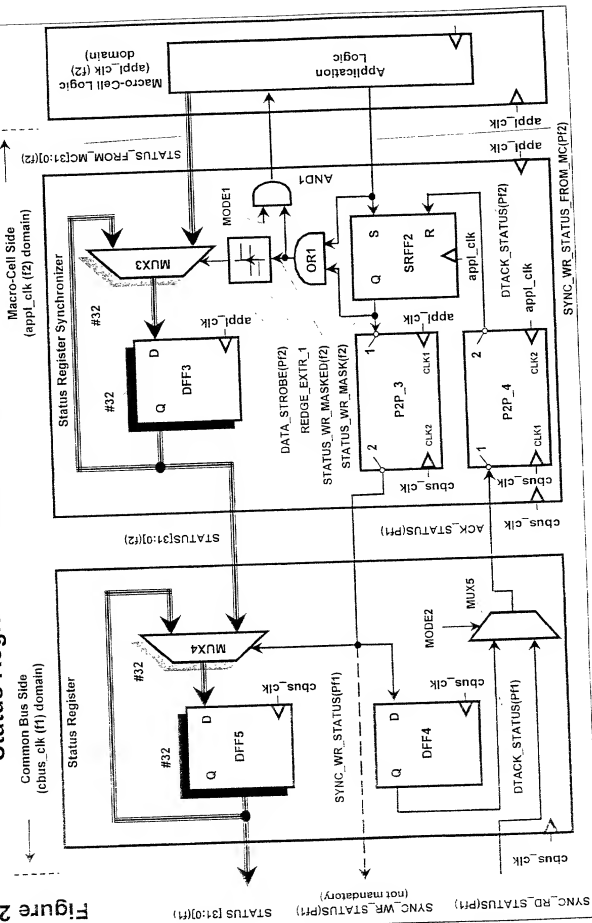
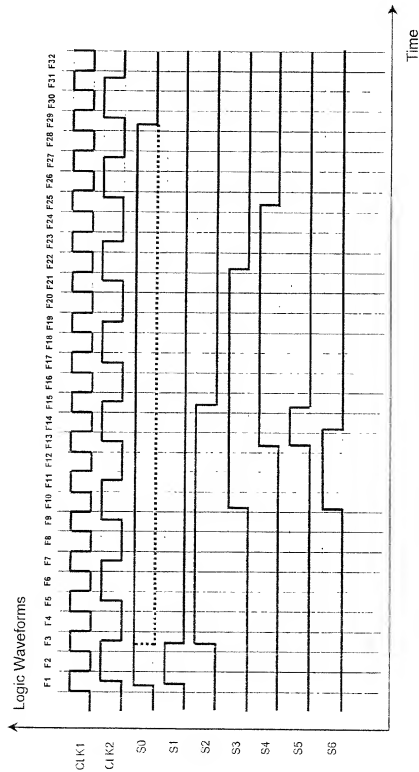




Figure 27

## Timing Diagram of Pulse to Pulse Synchronization Unit



## Advantages of Distributed Synchronization

Figure 28

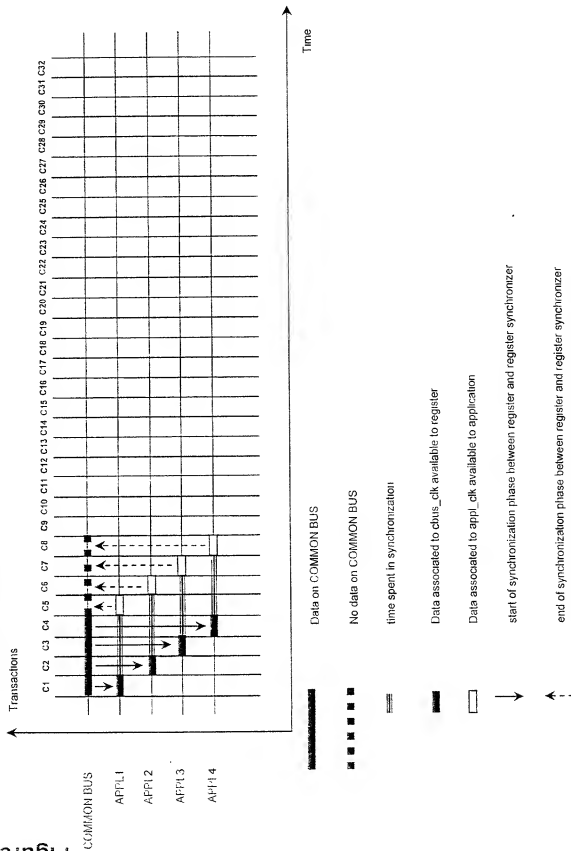


Figure 29

# EXTERNAL BUS AGENT DMI acting as Master

## Read Transaction from DMI PERIPHERAL 1

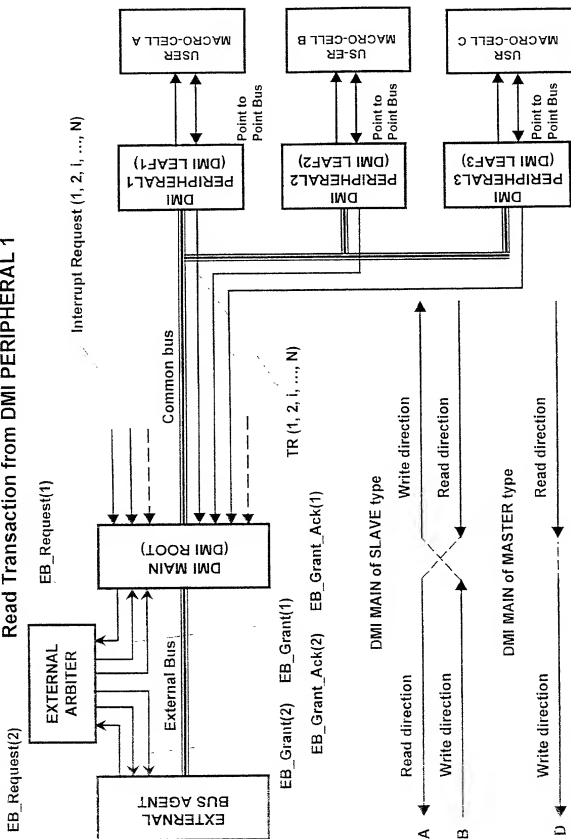
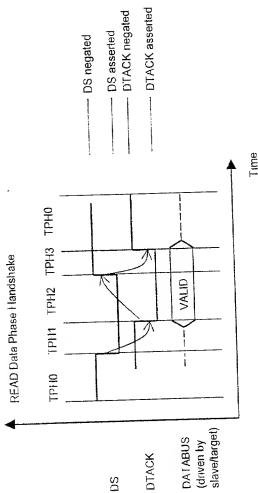


Figure 30

Asynchronous two phase handshake protocol: read



Prior Art

Figure 31

## Asynchronous two phase handshake protocol: write

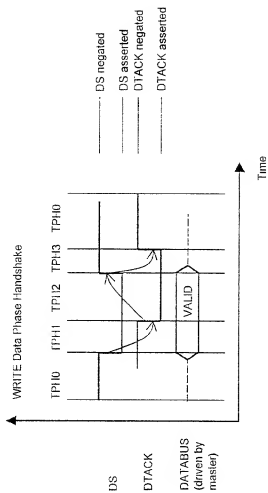
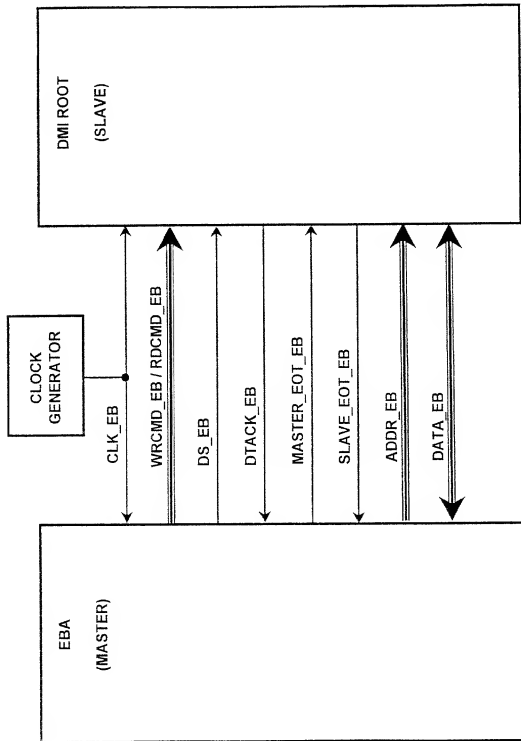


Figure 32

EBA-DMI ROOT interface  
MASTER: EBA  
SLAVE: DMI ROOT

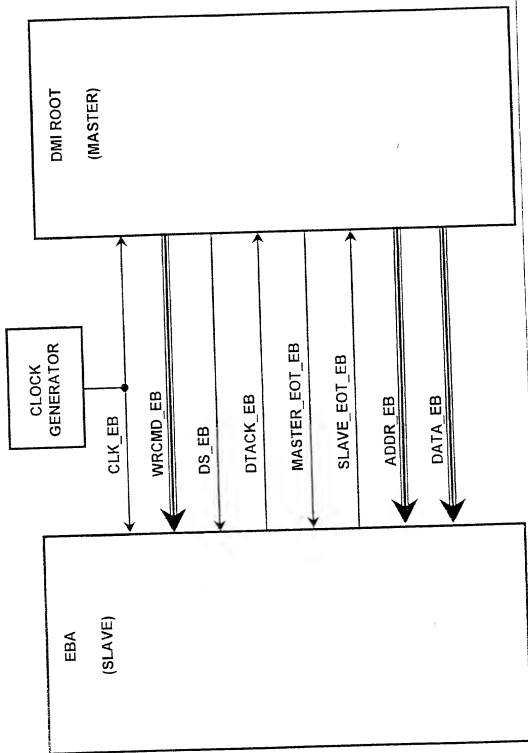


Prior Art



Figure 33

EBA-DMI ROOT interface  
MASTER: DMI ROOT  
SLAVE: EBA



Prior Art





Figure 36

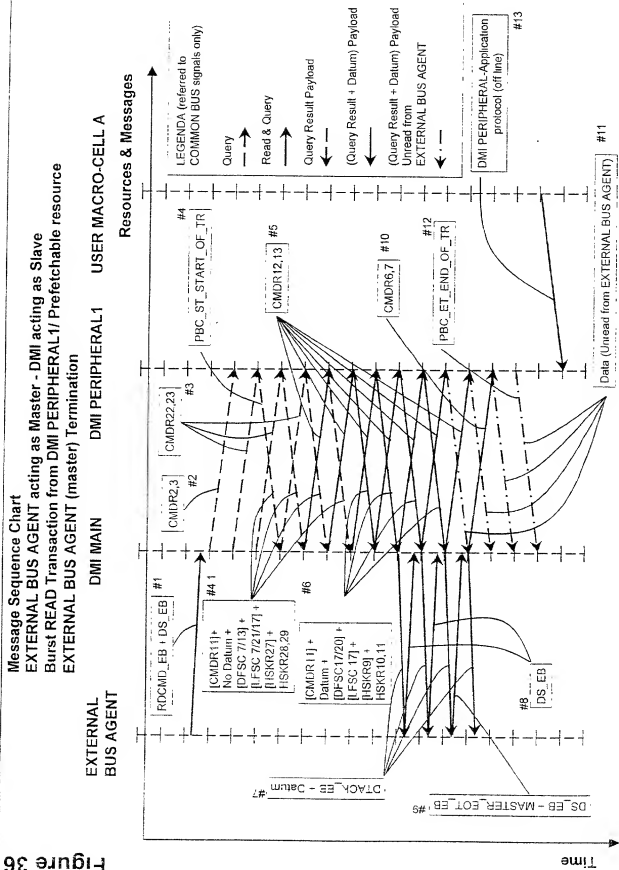


Figure 37

## Message Sequence Chart

EXTERNAL BUS AGENT acting as Master - DMI acting as Slave  
 Burst READ Transaction from DMI PERIPHERAL 1/ Prefetchable resource  
 DMI (slave) Termination

EXTERNAL  
BUS AGENT

DMI MAIN

DMI PERIPHERAL 1

USER MACRO-CELL A

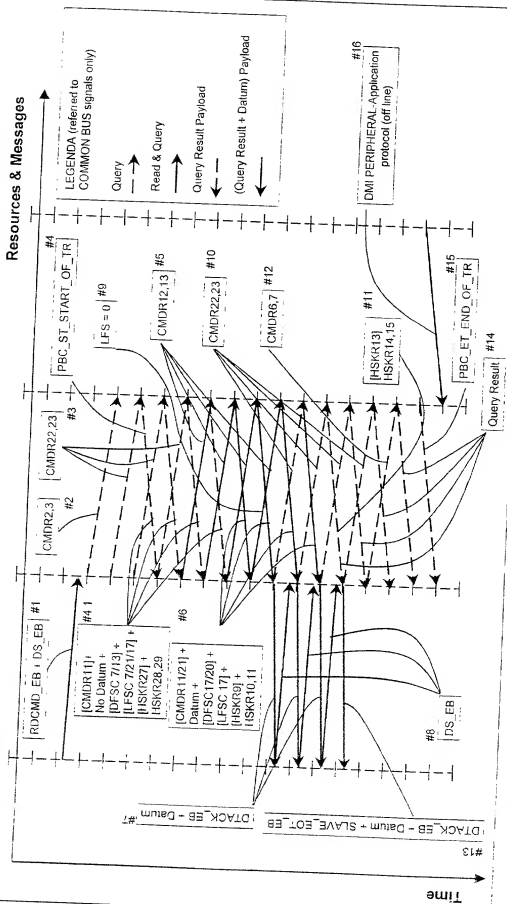


Figure 38

# DMI Slave Mode Overall Algorithm Representation Write Transaction from EXTERNAL BUS AGENT + Write Transaction to DMI PERIPHERAL

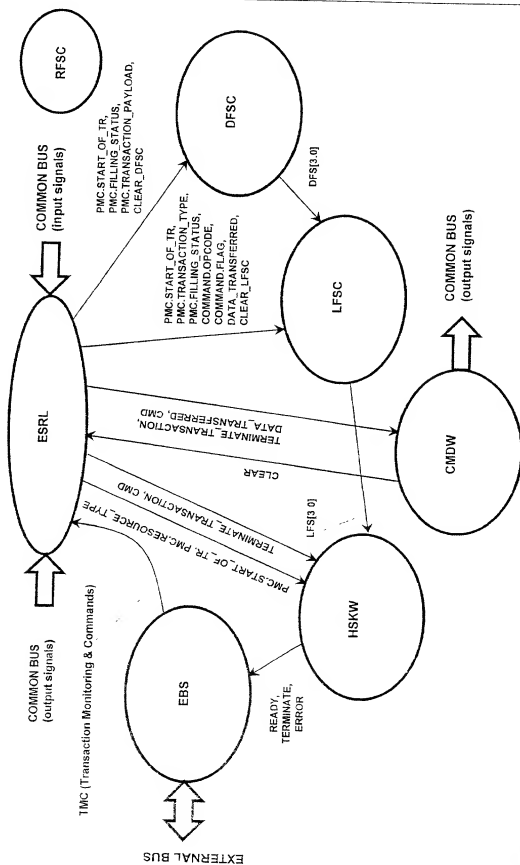


Figure 39

## Message Sequence Chart

EXTERNAL BUS AGENT acting as Master - DMI acting as Slave  
 WRITE Transaction to DMI PERIPHERAL 1/Prefetchable resource  
 EXTERNAL BUS AGENT (master) Termination

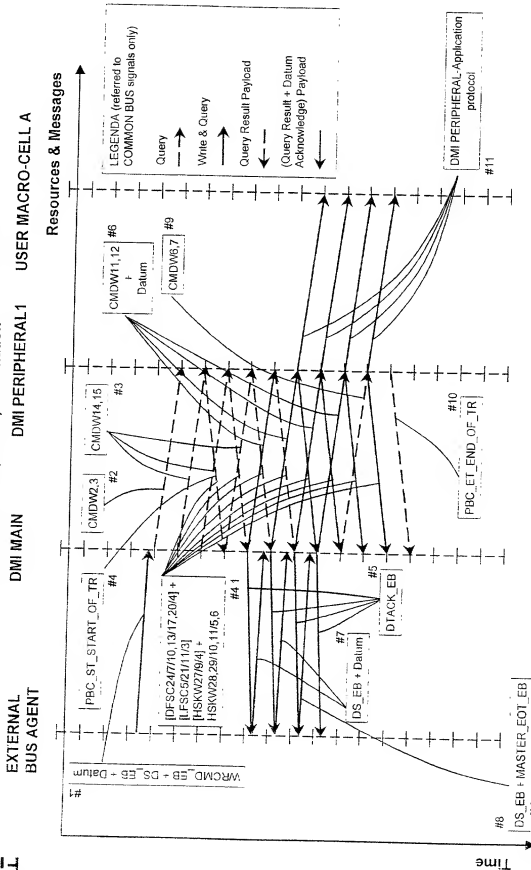


Figure 40

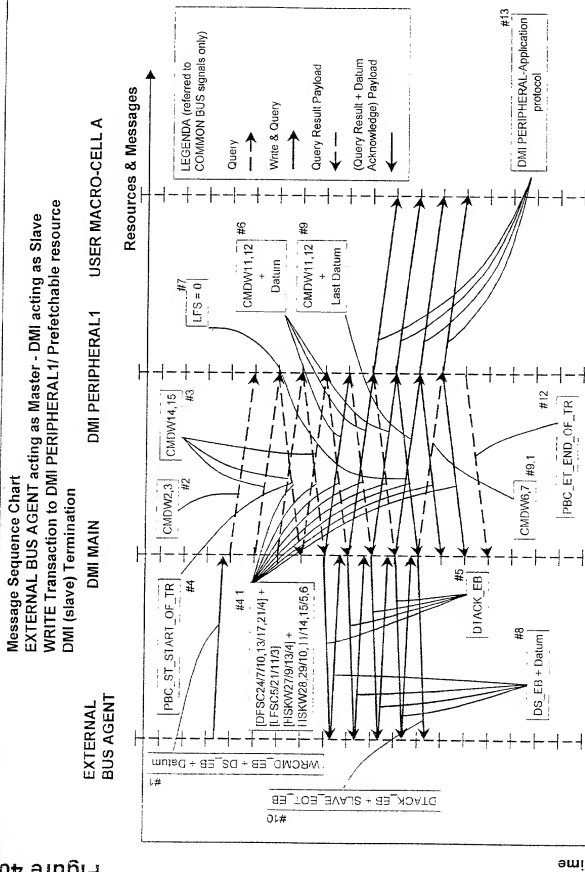






Figure 42

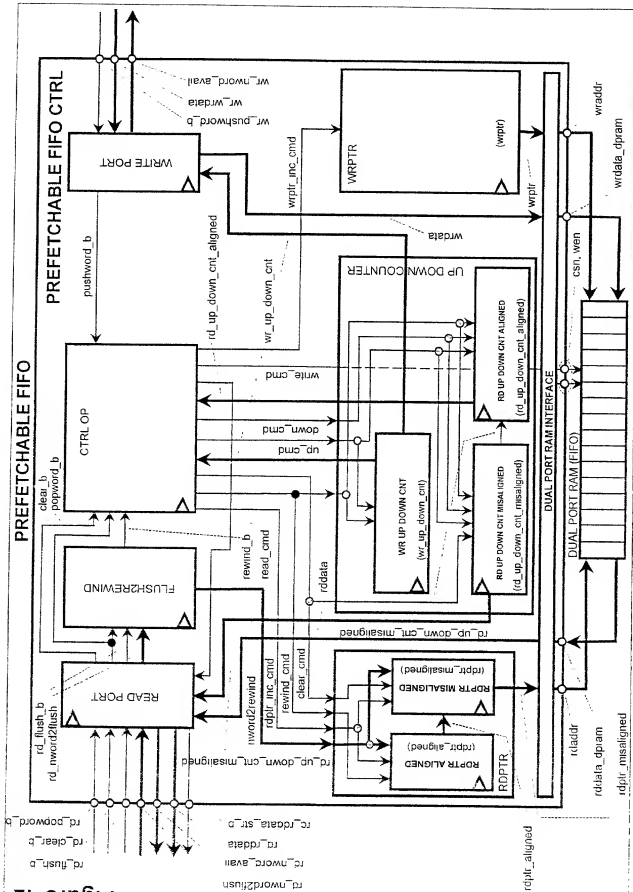


Figure 43

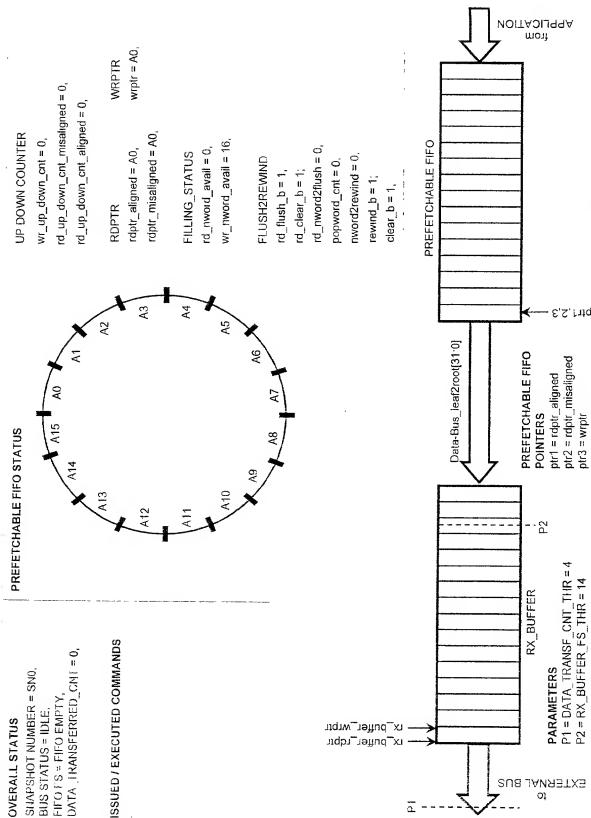


Figure 44

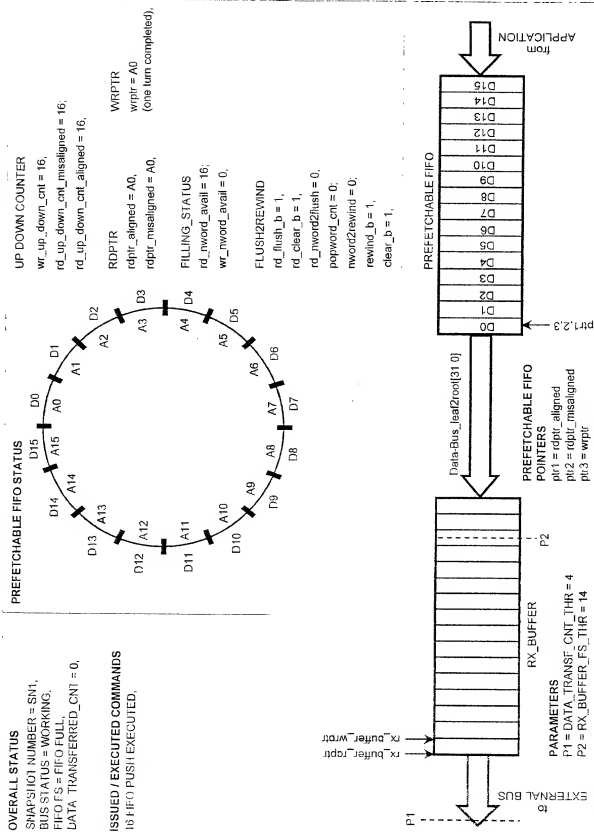


Figure 45

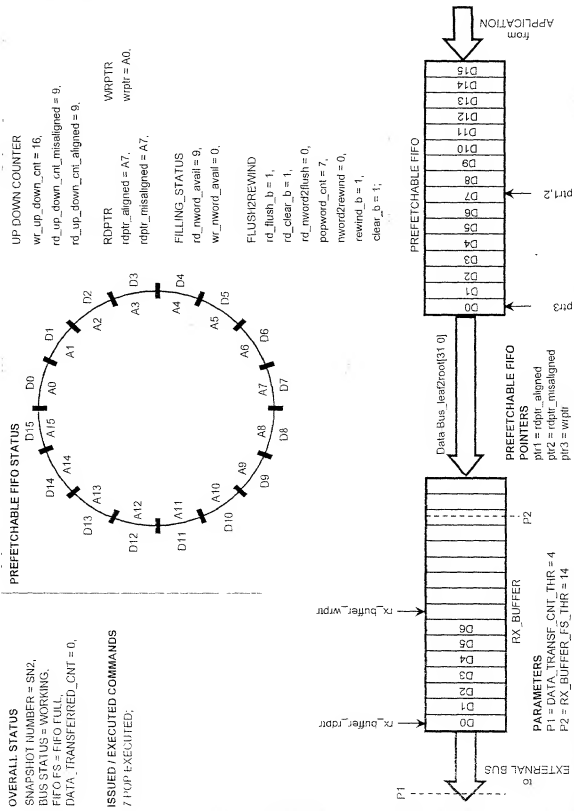


Figure 46

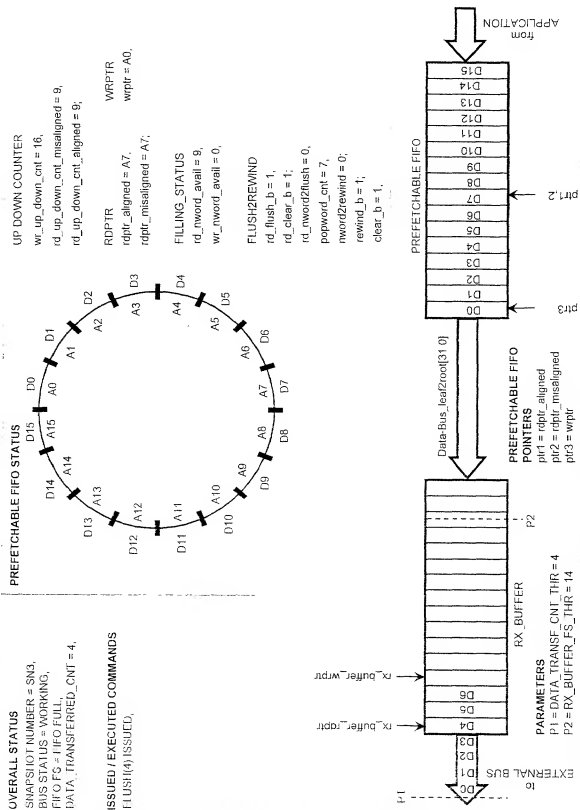


Figure 47

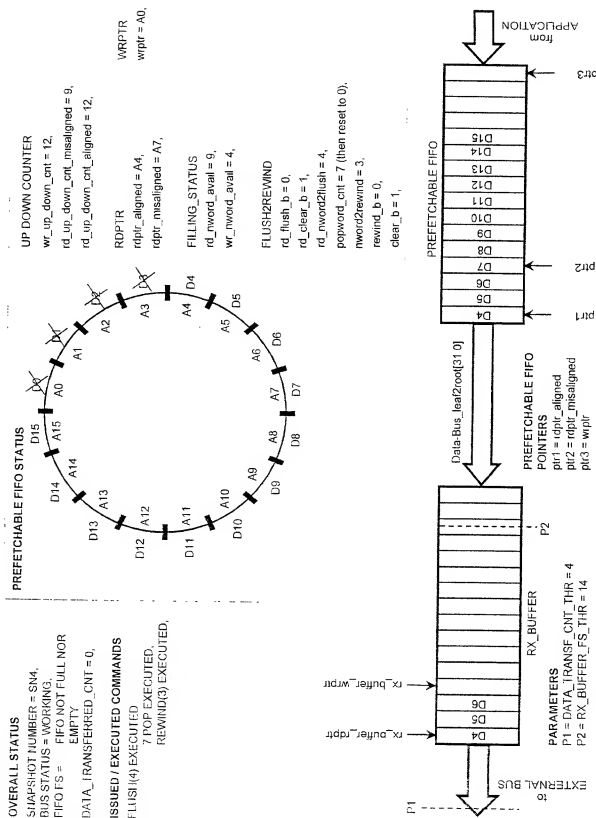


Figure 48

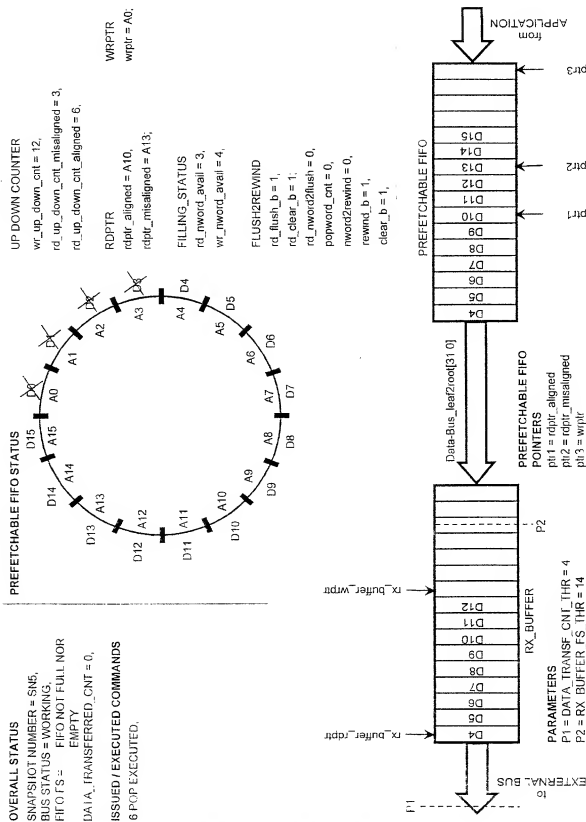




Figure 49

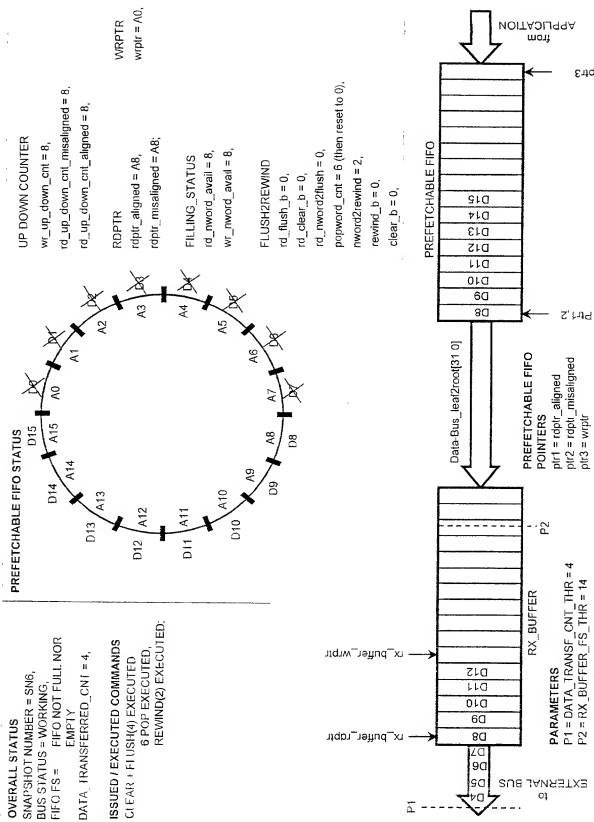


Figure 50

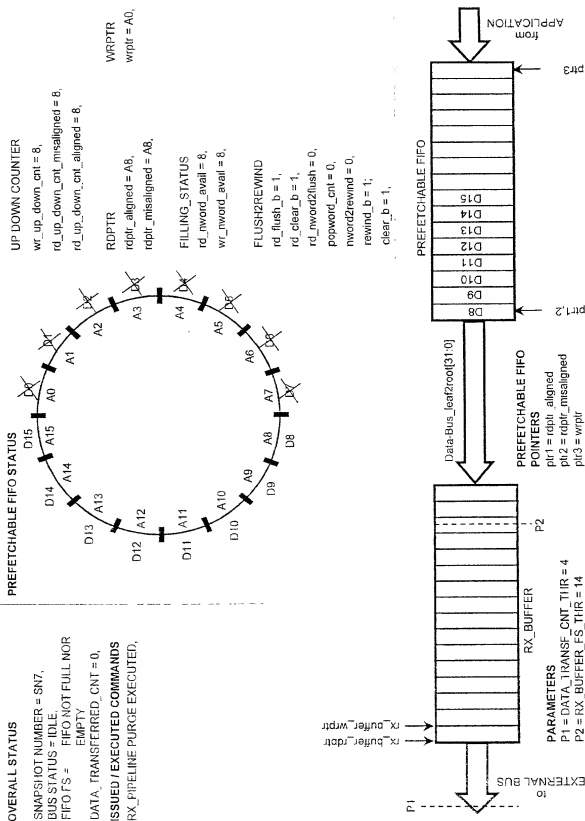


Figure 51

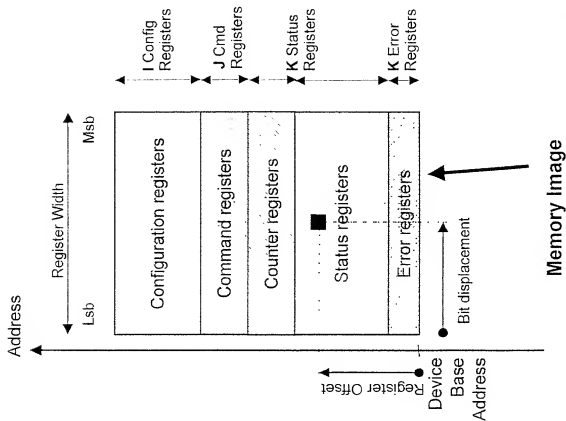


Figure 52

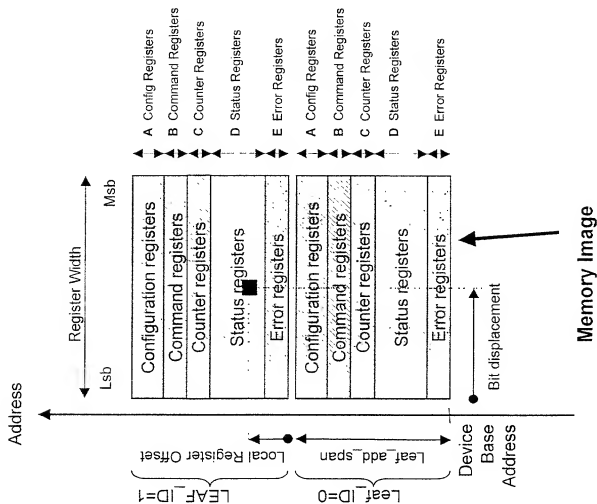


Figure 53

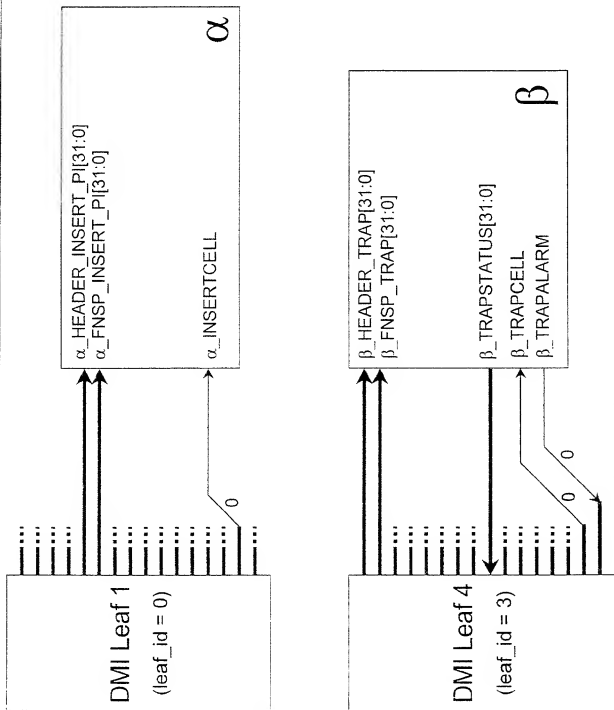


Figure 54

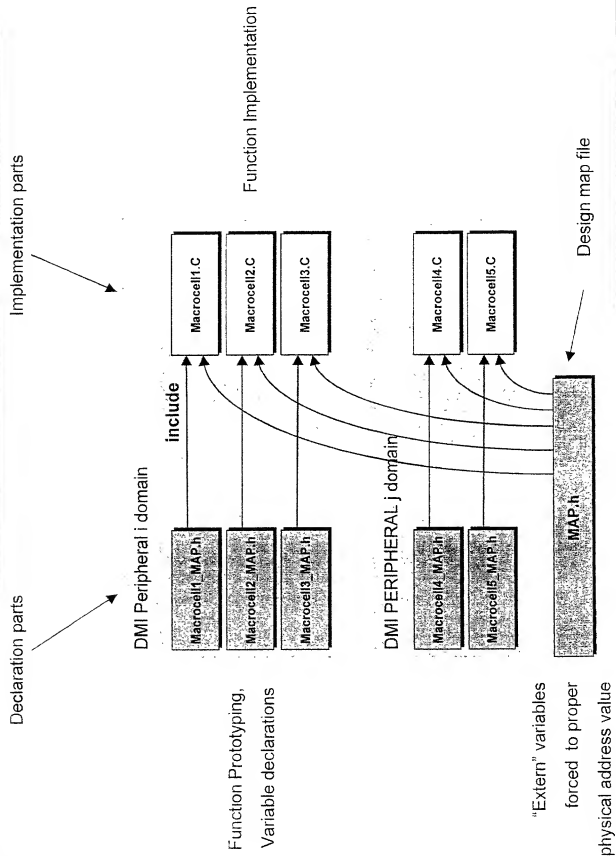


Figure 55

